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October 4, 2006

The Honorable Joseph J. Farnan, Jr.  
United States District Court  
844 King Street, Lockbox 27  
Wilmington, DE 19801

VIA ELECTRONIC FILING

Re: *Power Integrations, Inc. v. Fairchild Semiconductor International, Inc., et al.*,  
C.A. No. 04-1371-JJF

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Dear Judge Farnan:

As discussed during trial on Monday, enclosed is Fairchild's request for claim construction of certain issues.

Respectfully,

/s/ *Tiffany Geyer Lydon*

Tiffany Geyer Lydon

TLG/nml

Enclosure

173860.1

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Hon. Joseph J. Farnan, Jr.  
U.S. District Court  
District of Delaware  
844 King Street  
Wilmington, DE 19801

Re: *Power Integrations, Inc. v Fairchild Semiconductor International*  
USDC-D. Del. – C.A. No. 04-1371 JJF  
Request for Claim Interpretation

Dear Judge Farnan:

Fairchild requests claim construction issues discussed during Monday's proceedings. As discussed in the Court's Memorandum Order, the Court specifically deferred (1) "commenting on whether the term 'MOS transistor' excludes 'DMOS,'" and (2) "providing a construction of the disputed phrase ("within the substrate") beyond that which has been agreed to by the parties" "until such time as the DMOS issue is properly before the Court." [DI231 (3-31-06 Order at 9-10)] Fairchild now requests construction of those terms.

#### A. Prejudice

Fairchild requests claim construction to avoid the clear and extreme prejudice that will occur without a construction of the phrases "MOS transistor" and "within the substrate." Some 18 years ago, both claim terms were called out in the prosecution history and special emphasis was placed on them to avoid DMOS prior art. Today, in the final days of trial, Power Integrations has avoided any limitation based upon those statements. The law is clear that unequivocal statements disavowing prior art must be given full effect in the claims themselves.

The evidence at trial has shown that Power Integrations expressly disavowed coverage of DMOS devices during prosecution, that inventor Klas Eklund expressly stated in the subsequent '298 patent that the '075 patent was "not D-MOS" and that Fairchild engineers explicitly relied upon Power Integrations' disavowal during the development of the accused products. The evidence further shows that the accused Fairchild devices are DMOS devices as that term was understood when the patent was filed. It would be unjust to allow Power Integrations to expand its patents to recapture disavowed DMOS devices. Thus, although the word "DMOS" does not appear in the claims, each of those terms must be construed to exclude DMOS devices. Set forth below is Fairchild's claim construction position regarding the phrases "MOS transistor" and "within the substrate."



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**1. “MOS transistor” must be construed to exclude DMOS devices.**

| Claim Term      | Construction   |
|-----------------|--|
| MOS transistor: | “a metal-oxide-semiconductor transistor which excludes DMOS devices” |

“MOS transistor” should be interpreted to exclude the full scope of DMOS devices as expressly and intentionally disavowed by Power Integrations during prosecution. *See below* “A patentee may not state during prosecution that the claims do not cover a particular device and then change position and later sue a party who makes that same device for infringement.” *Spring Windows Fashions LP v Novo Indus., L.P.*, 323 F.3d 989, 995 (Fed. Cir. 2003). “Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers.” *Southwall*, 54 F.3d at 1576. Power Integrations clearly, deliberately, and repeatedly disavowed DMOS to have the ‘075 Patent granted and Fairchild is entitled to the full scope of that disavowal.

The term “MOS transistor” should be construed to exclude DMOS devices even though the term “DMOS” is not in the claims. *Spring Windows*, 323 F.3d at 995-996 (“We are unpersuaded by [patent owner]’s argument that the statements made during prosecution should be disregarded because the distinguishing features ‘were not and are not reflected in the claims’ and thus the statements simply constituted an error by the prosecuting attorney that should not be binding on the applicant.”). It also is appropriate to construe “MOS transistor” even though it only appears in the preamble because it gives meaning to the rest of claim 1 of the ‘075 Patent. “Terms appearing in a preamble may be deemed limitations of a claim when they give meaning to the claim and properly define the invention.” *In re Paulsen*, 30 F.3d 1475, 1479 (Fed. Cir. 1994). In *Paulsen*, the Federal Circuit noted that although the term “computer” only appeared in the preamble, it “breathes life and meaning into the claims and, hence, is a necessary limitation to them.” *Id.* Given the prosecution history, where Power Integrations excluded DMOS from “MOS transistor,” it is necessary to construe the term to incorporate the disavowed scope into the claim.

**2. “Within the substrate” must be construed to exclude subsequently doped regions.**

| Claim Term            | Construction   |
|-----------------------|--|
| Within the substrate: | “within the physical material on which a transistor or microcircuit is fabricated and not within subsequently doped regions” |



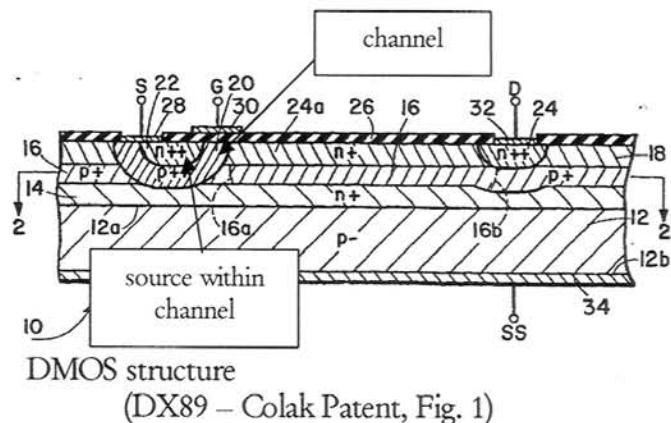
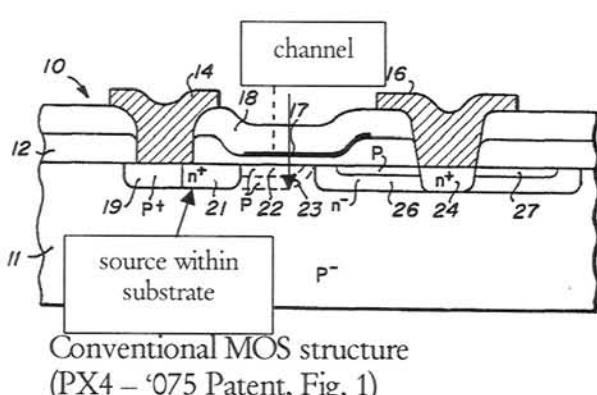
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During prosecution of the '075 Patent, when faced with the Colak reference, cited by the examiner, Power Integrations distinguished over that reference as follows:

Claim 19 [which issued as claim 1] also provides for a pair of laterally spaced source and drain contact pockets within the substrate as is customary for conventional MOS transistors and is thus, distinguished from DMOS devices which require a higher threshold voltage.

[See DX 201 (Amd (4/7/88), p. 6 (emphasis in original))] In this passage, Power Integrations distinguished all *DMOS devices* from conventional MOS on the basis that in conventional MOS transistors the source is “within the substrate.” The applicant added the phrase “within the substrate” to its claims in order to overcome the DMOS structure disclosed in the Colak reference in which the source is entirely within a subsequently doped channel region rather than within the substrate. [See DI 167 at Gwozdz Decl., Exh. A, ¶¶ 27-37] The difference is readily apparent from a simple comparison of the figures in the '075 Patent and the Colak reference:



Power Integrations similarly distinguished the conventional MOS structure from Colak's DMOS structure on the basis that in the conventional MOS device the substrate forms the channel region through which current flows from the source to the drain:

Claim 19 [which issued as claim 1] further provides for a substrate having a surface, and insulating layer on the surface of the substrate covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and a gate electrode on the insulating layer electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region. *Thus, claim 19 [which issued as claim 1] is limited to a MOS or MOSFET structure, while Colak shows a D-MOS device.*



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[DX102 (Amd after Final (8/12/88), p. 3)]. In a DMOS structure the subsequently doped body region in which the source pocket is formed also forms the channel of the device. [See DI 167 (Gwozdz Decl., Exh. A, ¶¶ 26-29)]

It is clear from the above passages that “within the substrate” means “within the physical material on which a transistor or microcircuit is fabricated and not within subsequently doped regions.” The propriety of this construction is two-fold. First, the Court has construed substrate as “the physical material on which a transistor or microcircuit is fabricated.” Second, Power Integrations’ explicitly added the language “within the substrate”—even underlining that language in its communication to the examiner—to distinguish over Colak which has a source within a subsequently doped channel region. Equally important, Power Integrations simultaneously cancelled the first 18 claims that lacked this limitation. Power Integrations now attempts to render its “within the substrate” limitation virtually meaningless by construing any doped region, including the DMOS p-body diffusion, as part of the substrate. In other words, Power Integrations is attempting to recapture the scope it relinquished during prosecution by incorporating the p-body region of a DMOS structure into the term “substrate.” With such a construction, Power Integrations will argue that forming a pocket and channel in a p-body region is the same as forming a pocket directly “within the substrate,” which eviscerates the reason it gave during prosecution for distinguishing Colak. If “substrate” could include such subsequently formed or doped regions, as Power Integrations’ construction implies, then the claims would not be distinguished from Colak.

Necessarily, it follows that “within the substrate” simply *cannot* mean placement within a subsequently doped region, as Power Integrations expressly disavowed such scope. It is well-settled that “all express representations made by or on behalf of the applicant to the examiner to induce the patent grant,” limits the interpretation of the claims “so as to exclude any interpretation that may have been disclaimed or disavowed during prosecution in order to obtain claim allowance.” *Standard Oil Co v American Cyanamid Co*, 774 F. 2d 448, 452 (Fed. Cir. 1985) (interpretations disavowed during prosecution are excluded from claim coverage); *see also Ekdian v Home Depot*, 104 F.3d 1299, 1303-1304 (Fed. Cir. 1997) (disavowal during prosecution of patent may result in narrowing of claim scope and can “also” create an estoppel and preclude infringement under the doctrine of equivalents).

Beyond the clear disavowal of claim scope during prosecution of the ‘075 Patent, in a later patent (U.S. Patent 5,146,298), Klas Eklund once again clearly repeated that the ‘075 patent *did not even describe* DMOS, stating as follows:

An efficient and simplistic way to incorporate a thin layer lateral high voltage MOS transistor which constitutes a series combination of a normal MOS transistor (not D-MOS) and a double-sided JFET is described in U.S. Patent Number 4,811,075 issued to Klas H. Eklund for High Voltage MOS Transistors.

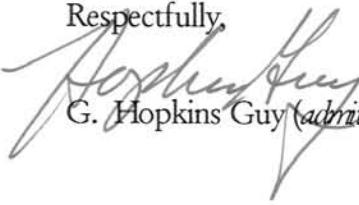


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[DX192 ('298 Patent, 1:37-45)]

Power Integrations repeatedly made explicit representations in the public record leading to the '075 Patent that the patent does not cover DMOS structures, in which the source and drain pockets are within subsequently doped regions. Fairchild relied upon Power Integrations' representations which clearly disavowed DMOS structures. [Testimony of C.K. Jeon (Trial Transcript, Day 2 at pp. 563-566] It would be manifestly unfair and contrary to the public notice function of the patent prosecution record to allow Power Integrations to now recover claim scope that it gave up during prosecution. *See Spring Windows Fashions LP v Novo Indus., L.P.*, 323 F.3d 989, 995 (Fed. Cir. 2003) ("A patentee may not state during prosecution that the claims do not cover a particular device and then change position and later sue a party who makes that same device for infringement."); *Southwall Techs., Inc. v Cardinal IG Co.*, 54 F.3d 1570, 1581 (Fed. Cir. 1995) (stating that the patentee, having distinguished a prior art reference in arguments made to the PTO, "cannot now escape [the defendant's] reliance upon this unambiguous surrender of subject matter"); *Lemelson v General Mills, Inc.*, 968 F.2d 1202, 1208 (Fed. Cir. 1992) ("Other players in the marketplace are entitled to rely on the record made in the Patent Office in determining the meaning and scope of the patent."); *Vitronics Corp. v Conptronics, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) ("Competitors are entitled to review the public record, apply the established rules of claim construction, ascertain the scope of the patentee's claimed invention and, thus, design around the claimed invention."). Accordingly, the term "within the substrate" should be construed as set forth herein.

Respectfully,

  
G. Hopkins Guy (*admitted pro hac vice*)